# Characterization of Clean after Photoresist Removal from Wafers with Copper Pillars with Lead-Free Solder Caps

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## ABSTRACT

Opportunities for developing enabling packaging schemes are being pursued as part of device improvement strategies for electronic products. Processes such as embedded technologies in wafer level packaging and 3-D chip architecture schemes open up opportunities for realization of a variety of package configurations. As a result, there are many opportunities to impact both device performance and the processes used to create them.

In the area of electroplated solder applications, there has been widespread adoption of copper pillar bumps with lead free solder caps. As more data is gathered using this process, one area of growing interest is the characterization of polymer photoresist residue on the side walls of plated copper pillars with lead-free solder caps. As has been seen with other processes, cleaning challenges have increased in tighter pitch applications.

This paper will describe wet cleaning processes used today for copper pillar cleans, with special focus on characterization of the Cu pillar and solder side walls. Examples using several different photoresists and copper and solder configurations will be examined. Samples with differing copper/solder bump heights and pitches will be discussed. Cleaning and compatibility results will be shown.

## INTRODUCTION

Wafer level packaging, including the use of solder plated bumping technologies has been in use in FlipChip technologies for a number of years. Initially the solder bump was a lead-based solder. With the knowledge that lead is a toxin to people and should not be concentrated in landfills or other areas, an effort was made to remove lead from solder used in electronics. Legislation was introduced in Europe, Directive 2002/95/EC, to restrict the use of six hazardous materials, including lead, found in electronic products. All applicable products in the EU subsequently have been made RoHS compliant. By 2010, lead-free solder was implemented in high volume manufacturing in most devices in most countries around the world.

In addition to the challenge of removing lead from the solder, devices continued to shrink and functionality continued to increase. These changes brought forth additional problems, including the need to more tightly arrange the solder connections to allow form factor reductions while maintaining good performance.[i] The solution that has been implemented in electroplated processes is the use of plated copper forms, called pillars, with a small amount of tin-based lead-free solder on top. In some instances a barrier material, most commonly nickel, is plated between the two layers. The advantages of this configuration include (i) solder wetting of only the copper pillars after reflow which confines the spread of the solder cap in the *x,y* plane after reflow and (ii) the use of smaller solder caps which increase the robustness of the interconnection.

Higher density, tighter pitch Cu pillar technologies have allowed for some changes in the materials used to create them, relative to their all-solder predecessors. Although thick photoresist is still needed, opportunities have arisen for liquid negative and liquid positive resists, in addition to dry films. Historically, liquid, spin-on photoresists have been easier to strip than dry film laminated photoresists. In addition, positive photoresists have been easier to strip than negative photoresists. These facts have led to the perception that photoresist stripping should be easier compared to previous configurations in previous generations. However, as more data is gathered using processes with any of these resist types, challenges continue to be identified,[ii] one of which is

challenging photoresist stripping. One area of growing interest is the characterization of polymer photoresist residue on the side walls of plated copper pillars with lead-free solder caps. As has been seen with other spin-on positive photoresist processes including for example, redistribution line (RDL) cleaning processes, cleaning challenges have increased in tighter pitch applications. In RDL, cleaning challenges were increased as cleaning processes that were once taken for granted were now being applied to wafers with 10µm line/space and tighter pitches. Analogies can be found in the tight pitch copper pillar cleans and some issues have been observed previously.[iii]

This paper discusses characterization of electroplated Cu pillar wafers after the photoresist removal process and identifies and discusses some of the challenges. The analyses were carried out using standard techniques such as optical microscopy (OM) in bright field and fluorescence modes, as well as other techniques less standard in inspection and test areas in the fab, but used routinely in failure analyses, including scanning electron microscopy (SEM) in both top-down view and at a 45° angle.

**RESULTS AND DISCUSSION**

Copper pillar wafers with solder caps and coated with TOK MP112 photoresist were used to show the efficiency of photoresist strip solutions to remove the photoresist mold and organic residues from the wafer surface. Wafers were cleaved into coupons approximately 5cm x 5cm square for bench scale testing. The wafers had been produced according to the general process flow in Fig 1.

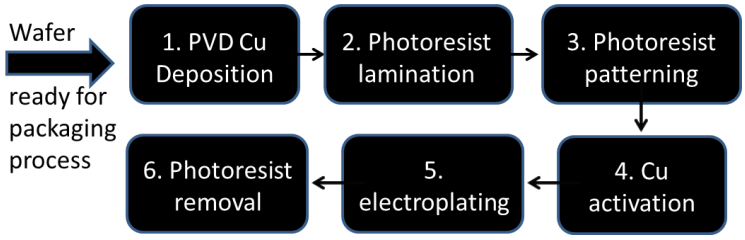



Figure 1. General Process Flow for Creation of Cu pillar wafers

All Cu pillar wafers were cleaved into coupons and cleaned in an immersion-based process at 60°C for 100 minutes, rinsed with deionized water and dried. A survey of Cu pillar cleaning results using two Dynastrip products and two competitive products was done to provide an increased understanding of the cleaning landscape. Images shown in Fig 2 (a-d, g-j) are cleaning results after the removal of 120µm thick TOK MP112 dry film. Fig 2(a–b, g-h)) show images after cleaning in Dynastrip product and (c–d, i-j) show images after cleaning in Competitive Product 1. Images shown in Fig 2(e-f, k-n) are cleaning results after the removal of 80µm of Asahi CX A270 dry film photoresist. Fig 2(e, k-l)) show images after cleaning in Dynastrip product and (f, m-n) show images after cleaning in Competitive Product 2. In each case, the wafer surfaces were clean. The compatibility with the solder is acceptable for typical processes.

Fig 3 shows a corresponding SEM image for each condition studied, obtained with the sample tilted to a 45° angle, allowing for a better view of the Cu pillar sidewall. In each case, a small amount of organic residue was found on each Cu pillar wall. This data showed that the Cu pillar residue issue was more widespread and suggested that all Cu pillar processes are potentially susceptible to residue, regardless of photoresist or remover used. Observing organic sidewall residue using conventional techniques may be a larger problem.

A second evaluation was performed in which two modes of optical microscopy were used, including bright field and fluorescence imaging to enhance detection of organic residue that might otherwise be undetected. The intensity of the fluorescence is low, and the microscope configuration must be adjusted to account for this. The

configuration includes a very high power light source, long exposure times, high magnification objectives, and correct placement of the focal plane in the same plane as the residue.

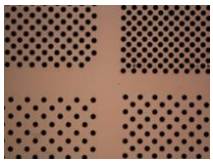
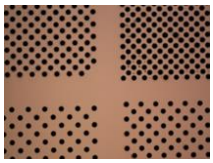
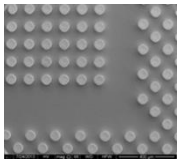
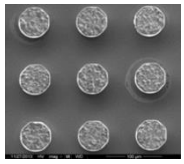
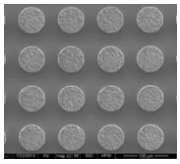
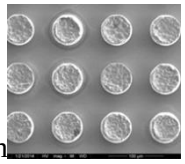
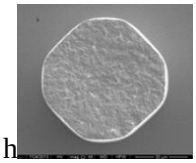
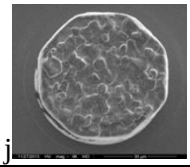
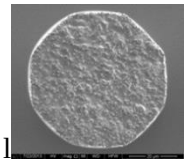
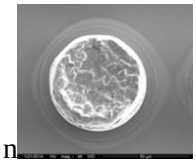
| Dynastrip AP7880C | Competitive Formulation 1 | Dynastrip AP7630 | Competitive Formulation 2 |
|---|---|---|---|
| a  | c  | e  | f  |
| b  | d  | N/A | N/A |
| g  | i  | k  | m  |
| h  | j  | l  | n  |

Figure 2. (a-d, g-j) Optical and SEM images of wafer surface after removal of TOK MP112 dry film using Dynastrip AP7880C or Competitive Formulation 1, (e-f, k-n) Optical and SEM images of wafer surface after removal of Asahi CX A270 dry film using a Dynastrip AP7630 or Competitive Formulation 2.

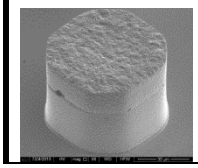
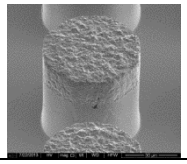
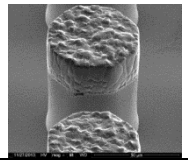
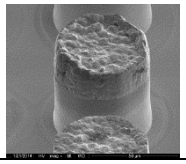
| Dynastrip AP7880C | Competitive Formulation 1 | Dynastrip AP7630 | Competitive Formulation 2 |
|---|---|---|---|
|  |  |  |  |

Figure 3. SEM Images at 45° tilt angle corresponding to the top-down images shown in Figure 2. In each case, some residue is found on the pillar sidewall, most commonly occurring at the interface between the Cu pillar and solder cap and that is not found during typical inspection.

Cu pillar wafers with 120µm of TOK MP112 dry film were cleaved and coupons were cleaned using a single wafer tool process.[iv] The wafer was processed at 120°C for 8 min. and then rinsed with water to remove the resist. Optical inspection was carried out. Images were obtained in both bright field and fluorescence mode. Fig 4 shows bright field and fluorescence images of Cu pillar wafers after strip.

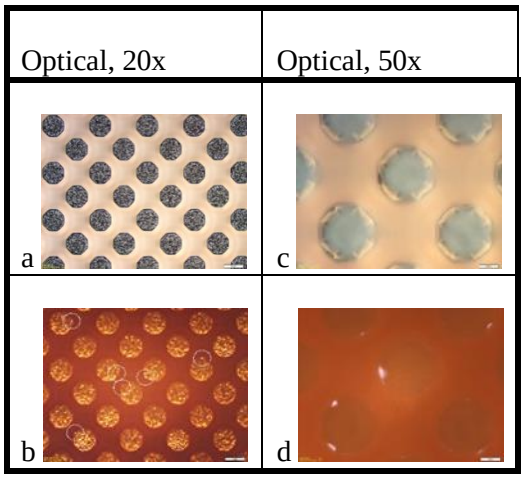



Figure 4 (a) Image of Cu pillar wafer, bright field, 20x magnification, (b) Image of Cu pillar wafer, fluorescence, 20x magnification, (c) Image of Cu pillar wafer, bright field, 50x magnification with focus on the Cu pillar/solder interface, (d) Image of Cu pillar wafer, fluorescence, 50x magnification

Some areas of fluorescence can be seen in Fig. 4(b, d) and indicate organic residue. Images obtained using SEM and shown in Fig 5 verify the presence of organic residue on the Cu pillar sidewalls. Fluorescence is a technique that could be optimized for Cu pillar sidewall residue, even when the images collected are plan view.

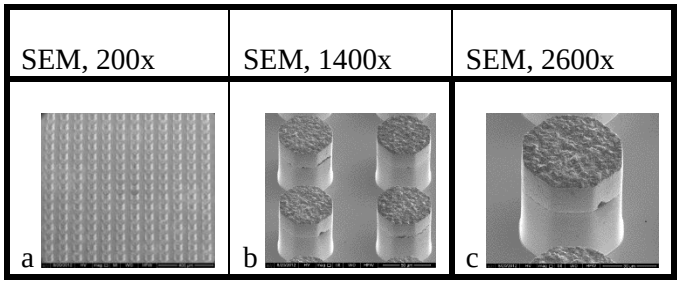



Figure 5. Images of Cu pillar samples after photoresist removal, tilted to 45° to better show the pillar side walls.

## CONCLUSIONS

Many things can contribute to residue on a sidewall, including the photoresist removal solution and process, the photoresist and plating solution used to manufacture the wafer and the smoothness of the Cu pillar, particularly at the interface. This study shows that challenges exist in the characterization of electroplated Cu pillar wafer surfaces after the cleaning step, using conventional bright field optical inspection. Fluorescence may be used to increase the sensitivity of traditional inspection techniques. Although fluorescence imaging is very capable of detecting small amounts of organic residue on Cu pillar wafers, it requires special care from the operator, making inspection over large areas difficult. Without a good solution to this problem, downstream problems affecting the viability of the interconnect may appear and which may be derived from the undetected presence of sidewall residue after photoresist removal.

[i] Patterson, D.S., Advancing Microelectronics, v39 (3), May/June 2012, pp18-24; Patterson, D.S., ChipScale Review, v16 (3), May/June 2012; Lee, M; *et al.*; 2009 IEEE Electronic Components and Technology Conference, "Study of Interconnection Process with Fine Pitch FlipChip", pp 720-723, 2009.
[ii] Pollard, KD; *et al.*; "Removal of TOK CR4000 Positive Photoresist in a Copper Pillar Bump Process", www.dynaloy.com, 2013.
[iii] Acra, T; *et al*;"Enabling Cleaning of Copper Pillar Wafers using a Stripper with Improved EHS Profile", www.dynaloy.com, 2014.
[iv] Peters, R; *et al*; "Single Wafer Resist Removal for Wafer Level Packaging with Improved Process Integration," IWLPC, 2013.